PRODUCT SPECIFICATION

MODEL: WD090HBM30AC-S0-07

<◇>PRELIMINARY SPECIFICATION

<◆>APPROVAL SPECIFICATION

	DESIGNED	CHECKED	APPROVED
CUSTOMER APPROVED			

	DESIGNED	CHECKED	APPROVED
SUPPLIER APPROVED	LCM RD 2018.03.31 王子勇	LCM RD 2018.03.31 王雷	LCM RD 2018.03.31 刘 欣

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REVISION STATUS

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TABLE OF CONTENTS

NO.	CONTENTS	PAGE
	REVISION STATUS	2
	TABLE OF CONTENTS	3
1.	GENERAL DESCRIPTION	4
2.	MECHANICAL SPECIFICATION	5
3.	PIN DESCRIPTION	6
4.	ELECTRICAL CHARACTERISTICS	7
5.	POWER ON/OFF SEQUEN	8---20
6.	OPTICAL CHARACTERISTICS.	21--23
7.	RELIABILITY TEST ITEMS	24--25
8.	GENERAL PRECAUTION	26
9.	PACKAGE DRAWING	27

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1. GENERAL DESCRIPTION

1.1 Introduction

XHS Display model WD090HBM30AC-S0-07 is a color active matrix thin film Transistor(TFT) liquid crystal display (LCD) that uses amorphous silicom TFT as a Switching device. This model is composed of a TFT LCD panel,a driving circuit and a back light system.This TFT LCD has a 9(16:9) inch diagonally measured active display area with WSVGA (720 horizontal by 1280 vertical pixel) Resolution.

1.2 Features

- 9 inch (16:9 diagonal) configuration
- 16.7M color by 6 bit + Hi -FRC input
- RoHS/Halogen Free Compliance

1.3 Applications

- **Automotive**

1.4 TFT LCD General information

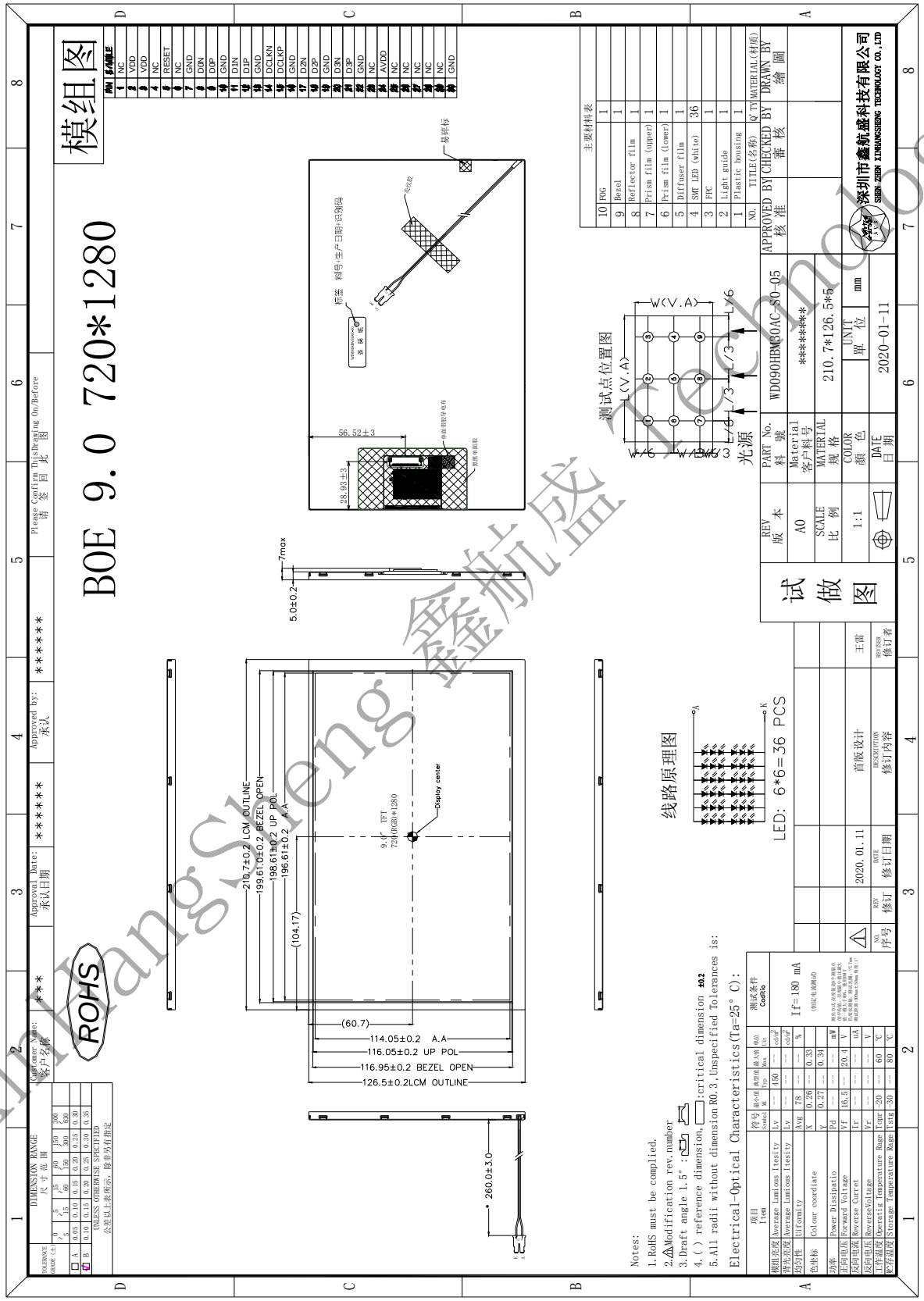
Item	Specification	Remark
Panel Size	9.0 inch(Diagonal)	
Resolution	720 x 3(RGB) x 1280	
Driver Method	A-Si TFT active matrix	
Active Area	144.048(H)x196.608(V)mm	
Dot Pitch	0.0528 (H)x 0.2175(V)mm	
Pixel Arrangement	RGB-stripe	
Module Size	126.5 (W) x 210.7(H) x5.1(D) mm	
Display Mode	Normally Black	
Display Color	16.7M	
Viewing Direction	ALL	
Interface	MIPI 4 lane	
Driving IC	SC7705	
Weight	TBD	g

1.5 Mechanical information

Item		Min.	Typ.	Max.	unit
Module size	Horizontal(H)	210.5	210.7	210.9	mm
	Vertical(V)	126.3	126.5	126.7	mm
	Depth(D)	---	5.1	5.3	mm
weight		**----**	(146)	**---**	g

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2. MECHANICAL SPECIFICATION



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3. PIN DESCRIPTION

MIPI Connector HRS Model Number :FH33-30S-0.5SH

No.	Symbol	Function	Remark
1	NC	NC	
2	VDD(1.8V)	Power for Digital Circuit	1.8V
3	VDD(1.8V)	Power for Digital Circuit	1.8V
4	NC	NC	
5	NC	No connection	
6	NC	NC	
7	GND	Power ground	
8	D0N	Negative MIPI differential Data inputs	
9	D0P	Positive MIPI differential Data inputs	
10	GND	Power ground	
11	D1N	Negative MIPI differential Data inputs	
12	D1P	Positive MIPI differential Data inputs	
13	GND	Power ground	
14	CLKN	Negative MIPI differential clock inputs	
15	CLKP	Positive MIPI differential clock inputs	
16	GND	Power ground	
17	D2N	Negative MIPI differential Data inputs	
18	D2P	Positive MIPI differential Data inputs	
19	GND	Power ground	
20	D3N	Negative MIPI differential Data inputs	
21	D3P	Positive MIPI differential Data inputs	
22	GND	Power ground	
23	NC		
24	AVDD	INPUT +10V	
25	NC		
26	NC	No connection	
27	NC	No connection	
28	NC	No connection	
29	NC		
30	GND	Power ground	

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4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	3.6	V
Analog supply voltage	AVDD	-0.3	15	V

4.2 TFT LCD MODULE

4.2.1 OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Supply Voltage	VDD	1.7	1.8	1.9	V
Power Supply voltage	AVDD	9.5	10	10.5	V

4. 3 Current Consumption

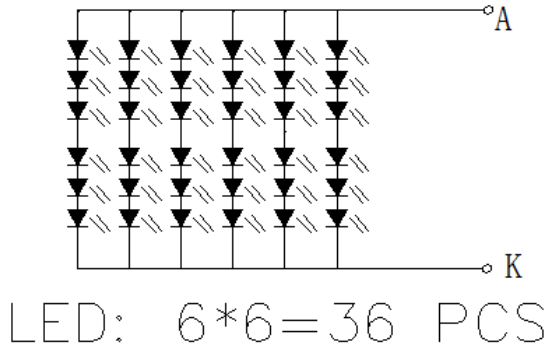
Symbol	Item	Min.	Typ.	Max.	Unit	Remark
IVDD	Digital Current	--	20	--	mA	VDD=1.8V
IAVDD	Power Supply voltage	--	20	--	mA	AVDD=10V

4.4 BACK LIGHT UNIT

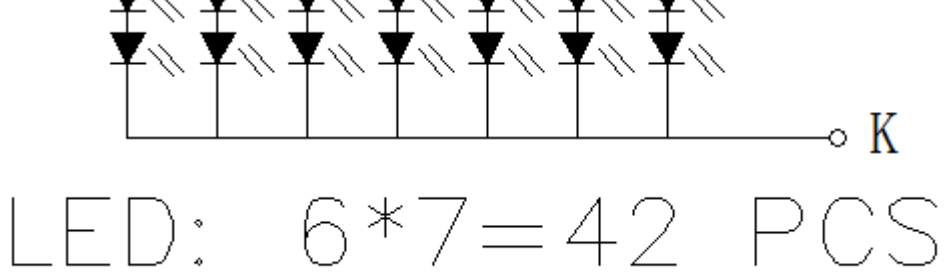
Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	ILED	160	180	200	mA	Total LED
Forward voltage	VF	16	18.0	19.2	V	IF=180mA
Reverse current	IR			50	μA	VR=5V,1LED
Power dissipation	Pd	2520			mW	Total LED
Peak forward current	IFP	150			mA	1LED
Reverse Voltage	VR	5			V	1LED

线路原理图



LED: 6*6=36 PCS



LED: 6*7=42 PCS

POWER SOURCE IOVCC, VCI CAN BE APPLIED AND POWERED DOWN IN ANY ORDER. IOVCC, VCI CAN BE POWERED DOWN IN ANY ORDER.

DURING POWER OFF, IF LCD IS IN THE SLEEP OUT MODE, IOVCC, VCI MUST BE POWERED DOWN MINIMUM 120MSEC AFTER NRESET HAS BEEN RELEASED.

DURING POWER OFF, IF LCD IS IN THE SLEEP IN MODE, IOVCC, VCI CAN BE POWERED DOWN MINIMUM 0MSEC AFTER NRESET HAS BEEN RELEASED.

NCS CAN BE APPLIED AT ANY TIMING OR CAN BE PERMANENTLY GROUNDED. NRESET HAS PRIORITY OVER NCS.

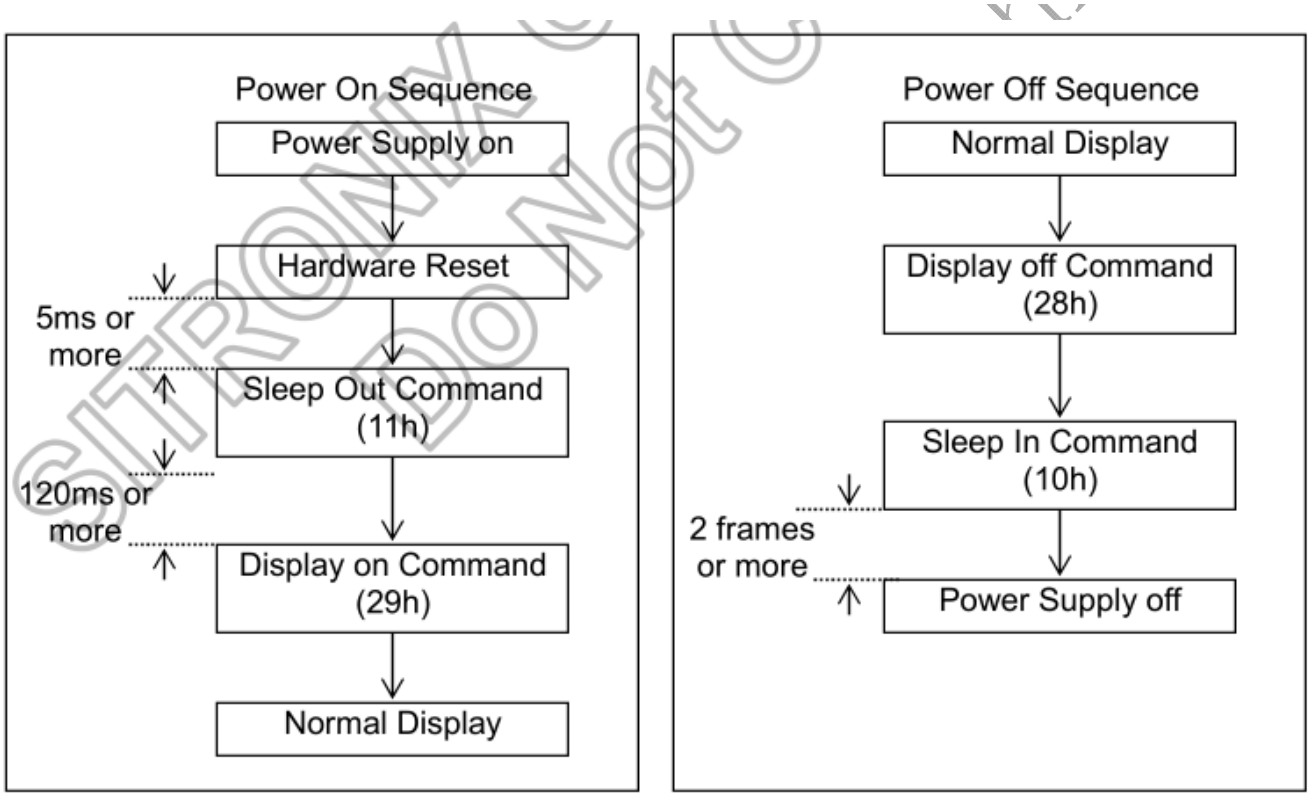


Figure : The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

5.0.1 Case 1: RESX line is held high or unstable by host at power on

RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

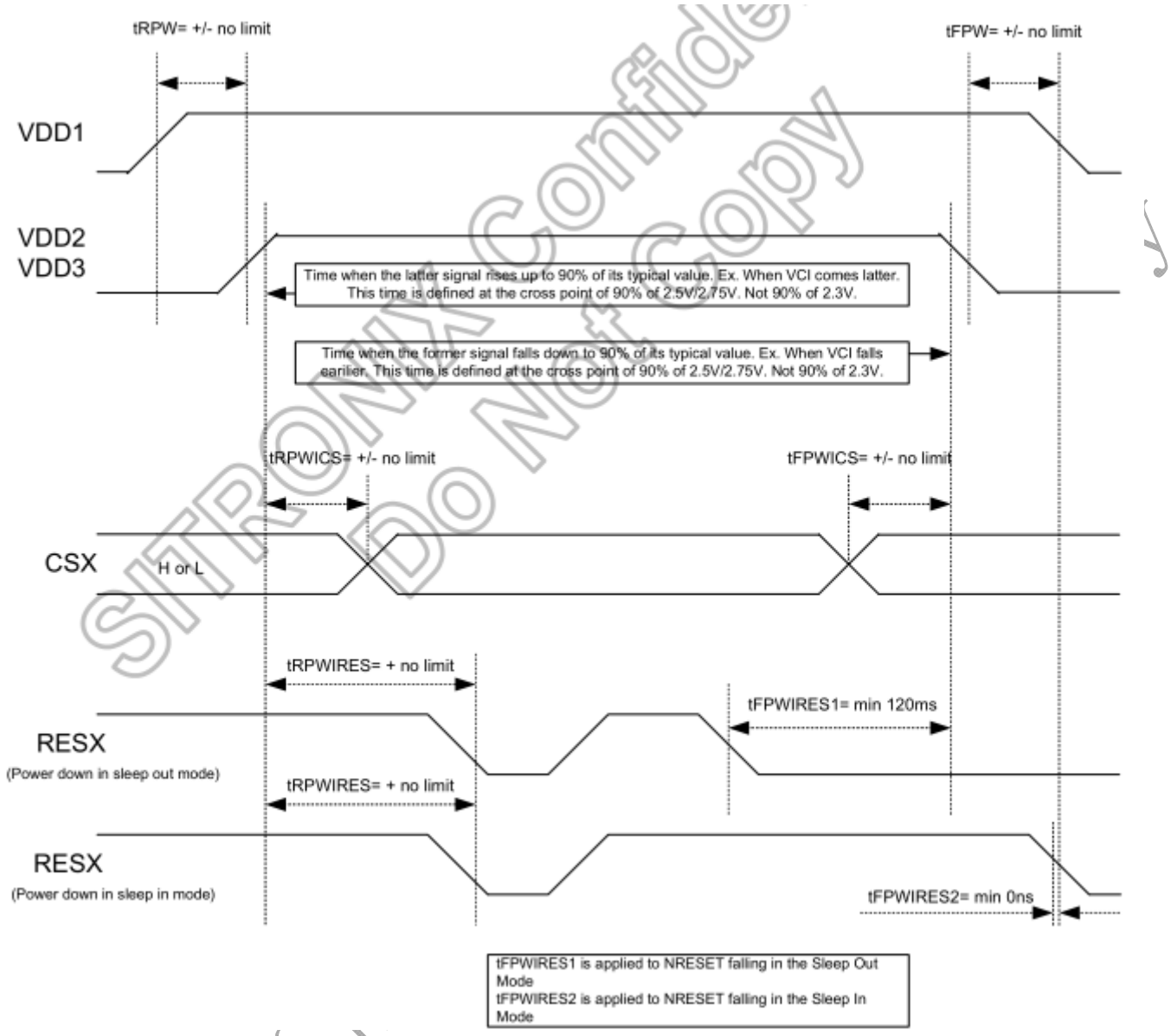


Figure : Case 1: RESX line is held high or unstable by host at power on

5.0.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.

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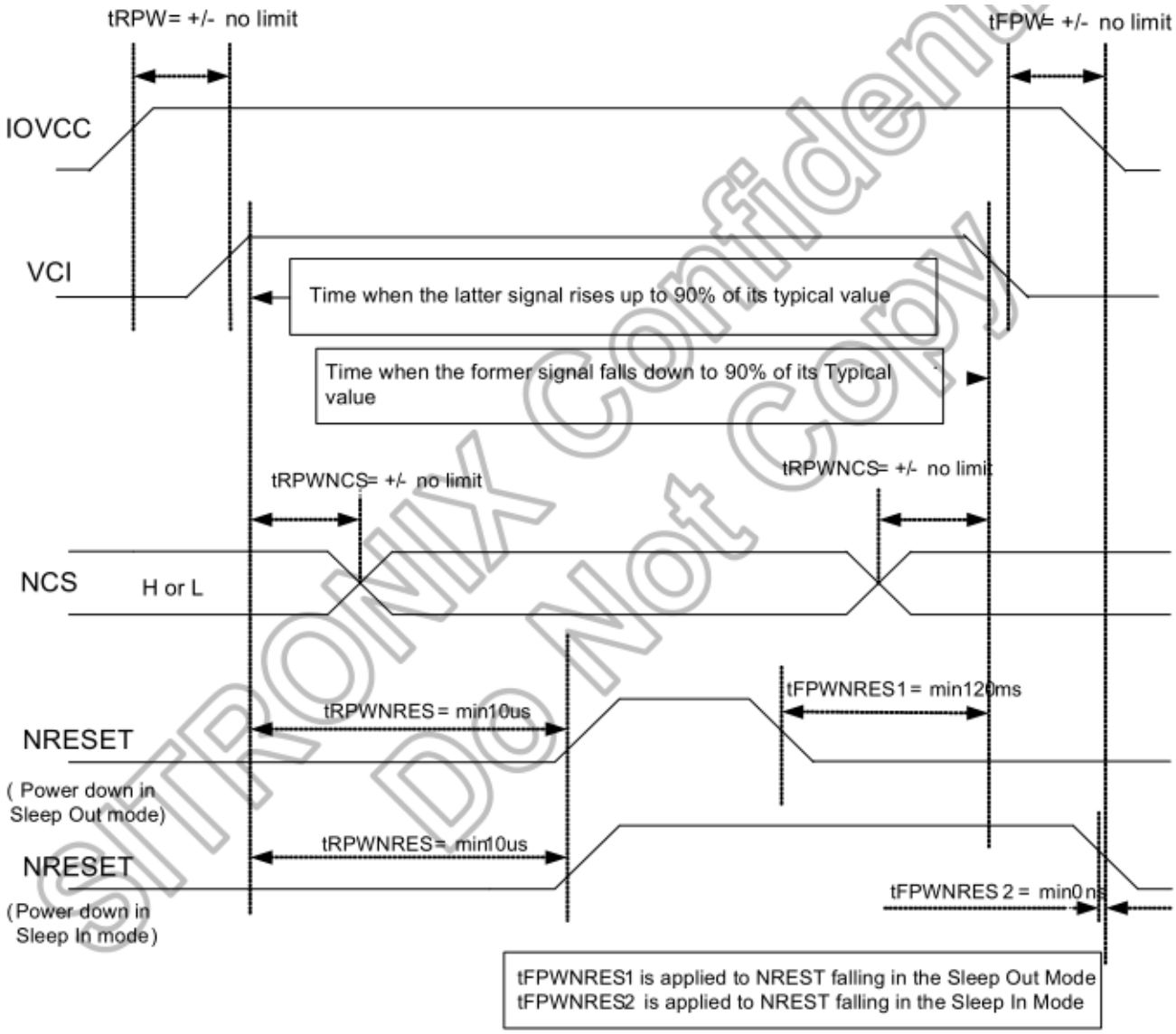


Figure: Case 2: RESX line is held low by host at power on

5.0.3 Power levels definition

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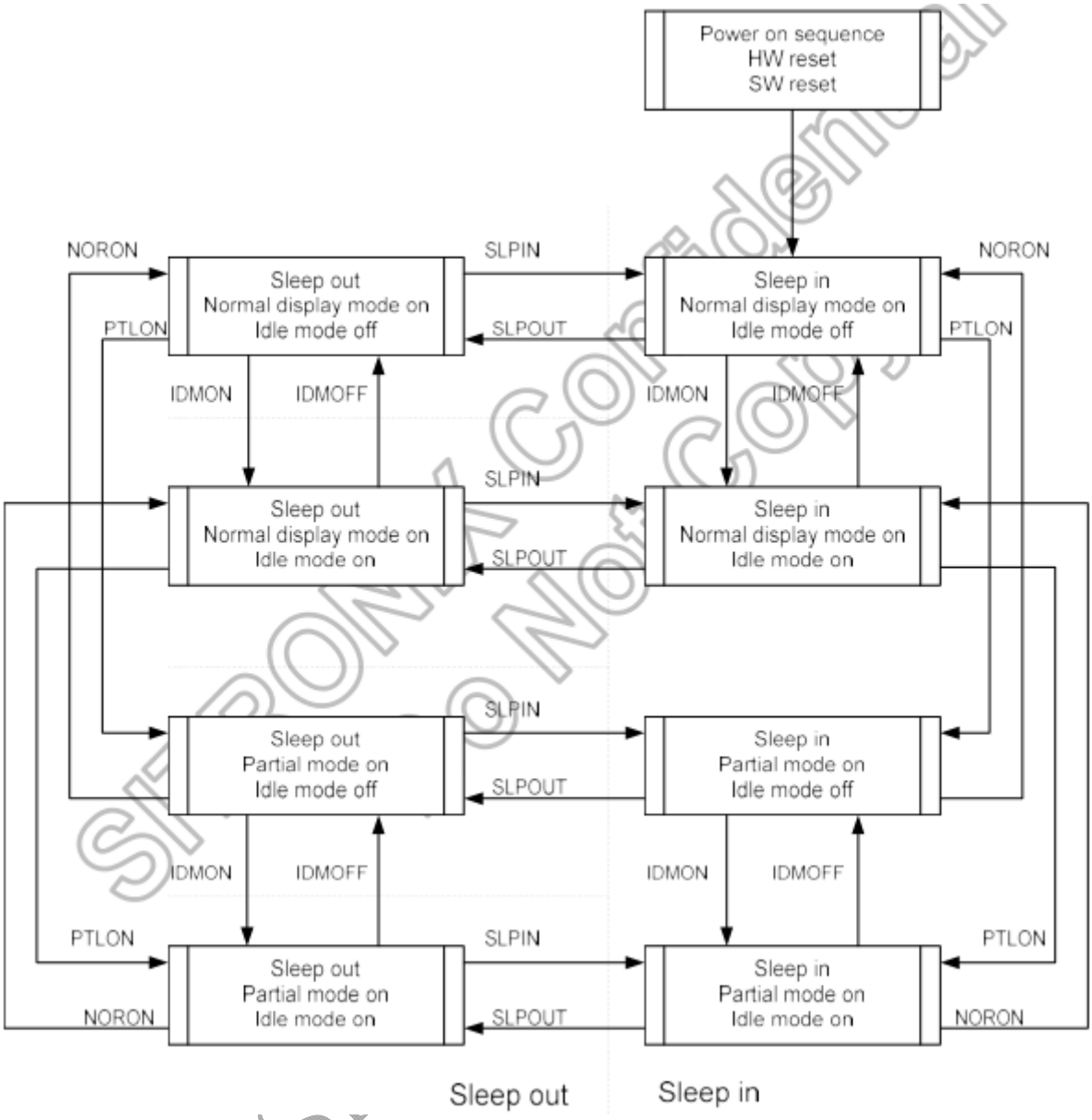


Figure: Power flow chart for different power modes

5.1 DSI DC Characteristics

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LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

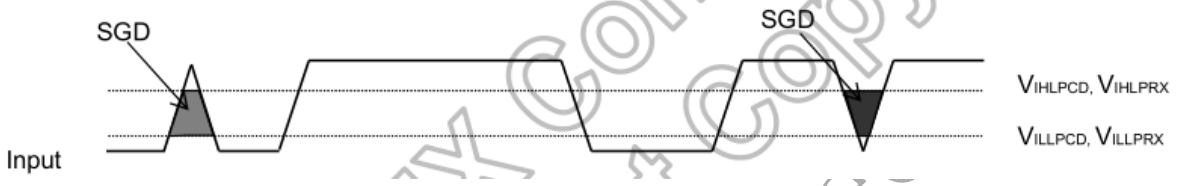


Figure: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

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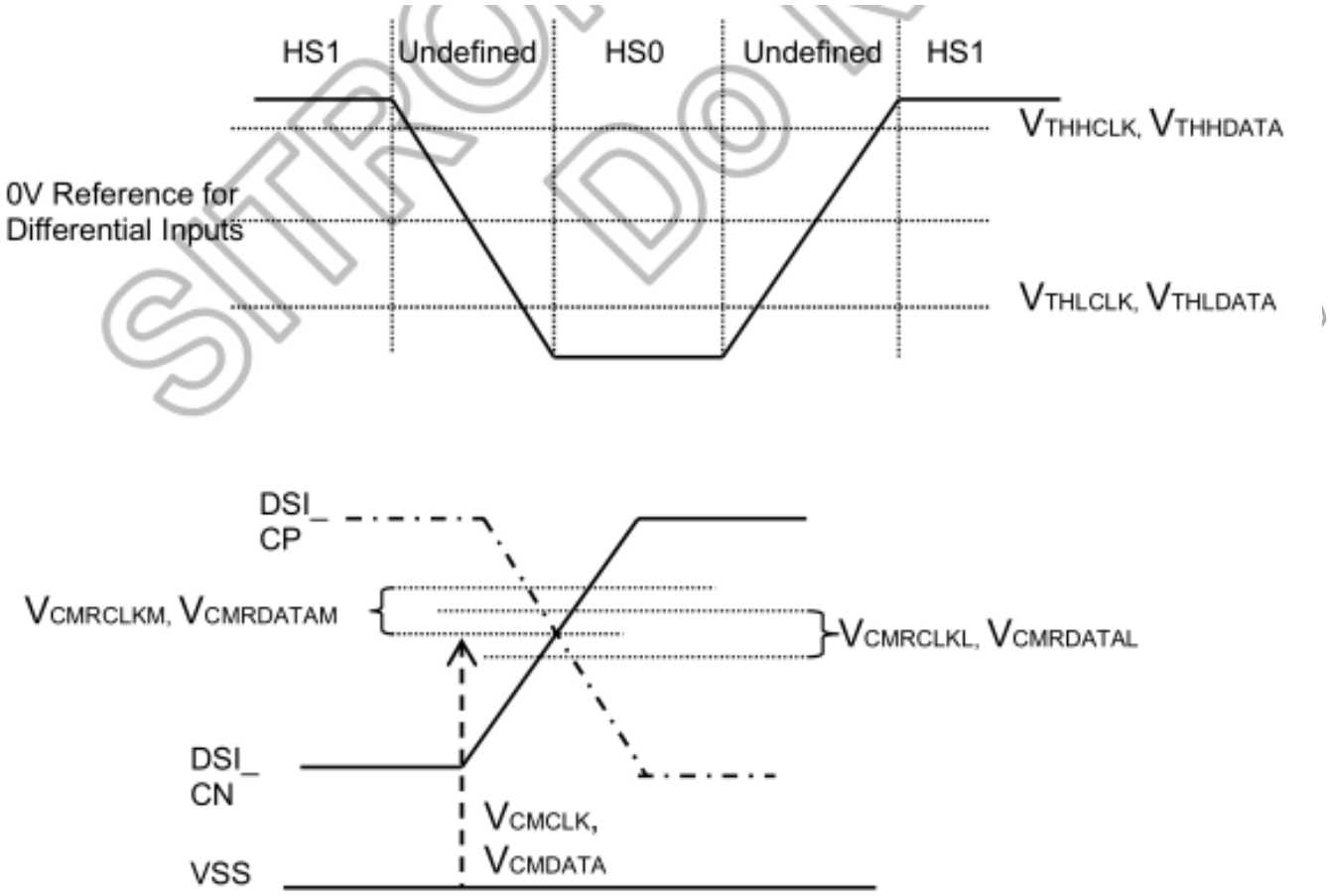


Figure : Differential voltage range and Command mode voltage

5.2 DSI Interface Timing Characteristics

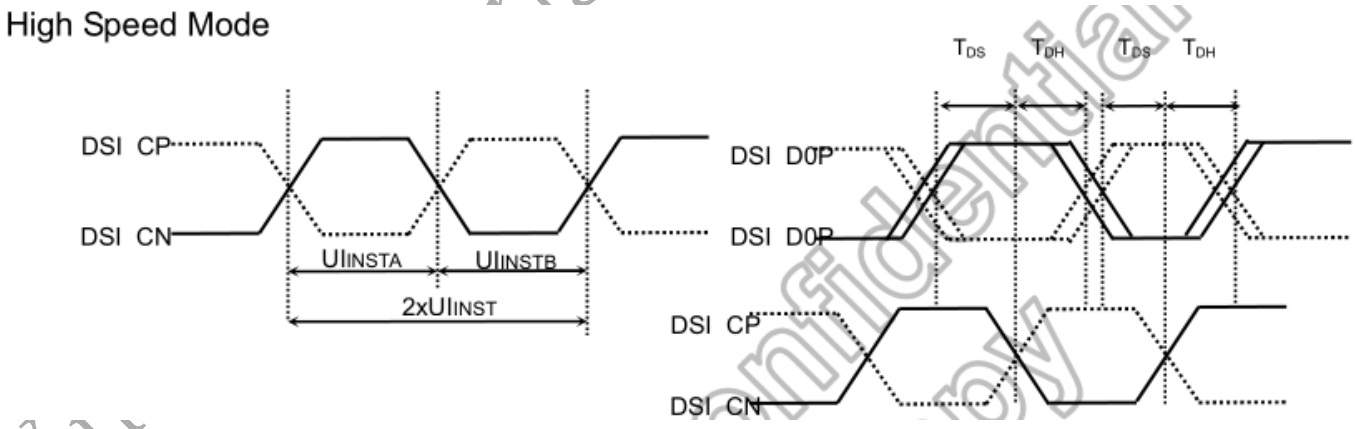


Figure : DSI clock timing Characteristics

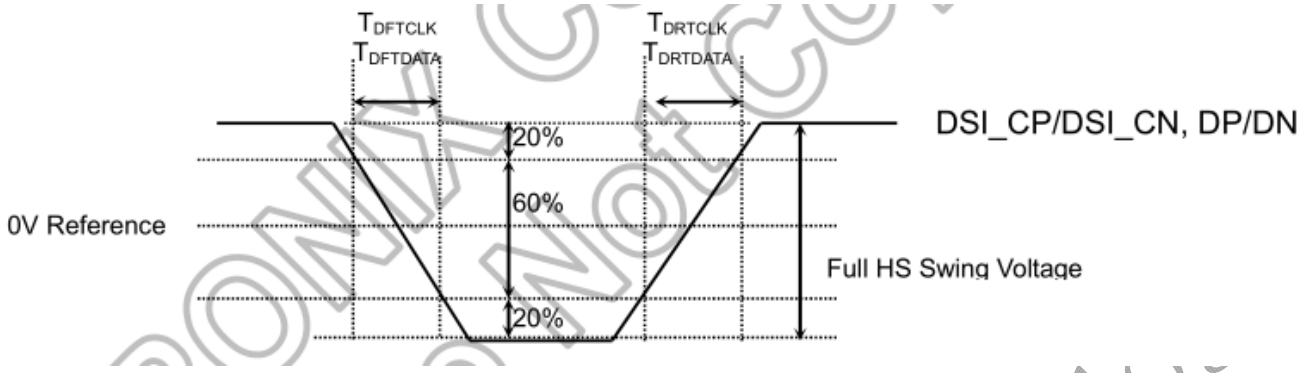


Figure : Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xU_{INST}	TBD	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table : DSI High Speed Mode characteristics

Low Power Mode

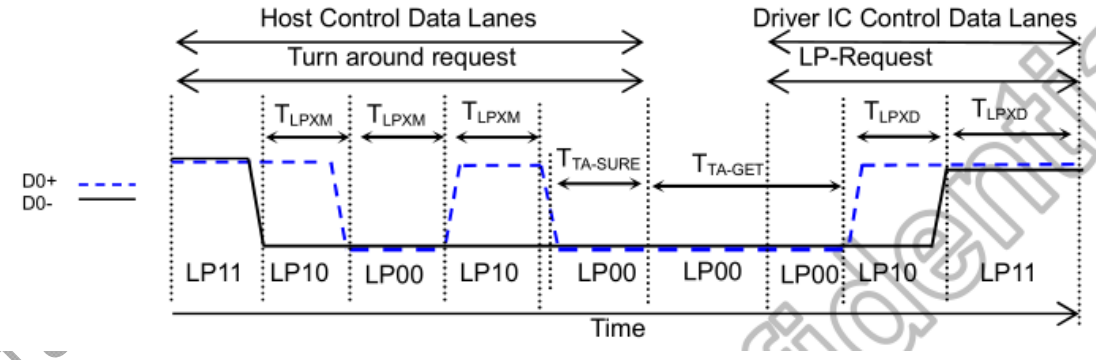


Figure : BTA from HOST to Display module Timing

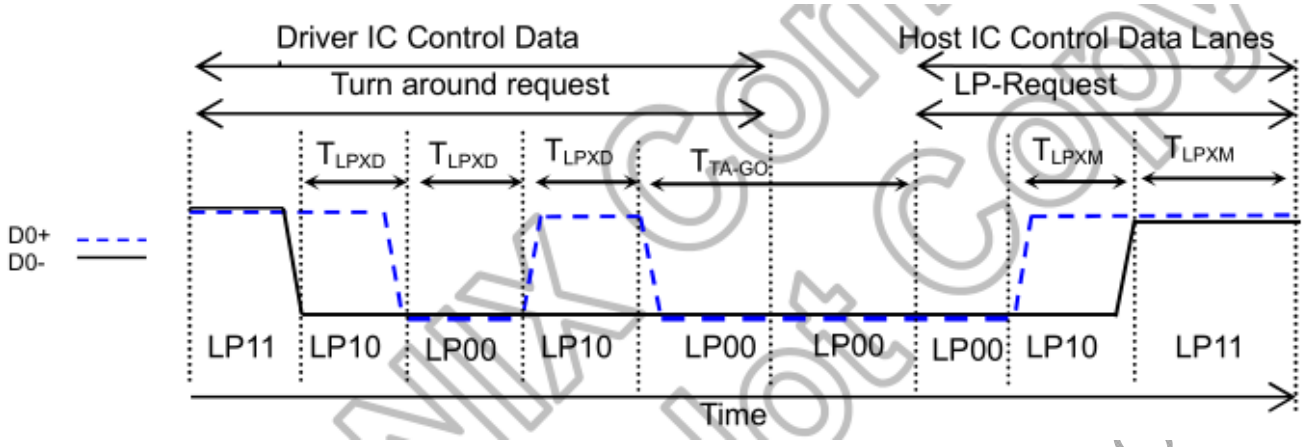


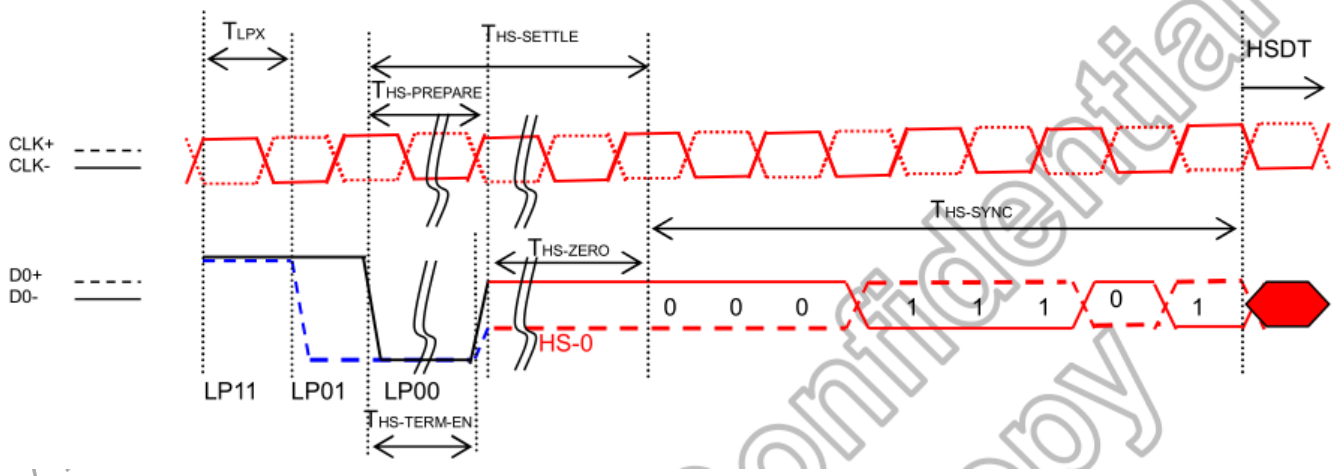
Figure : BTA from Display module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

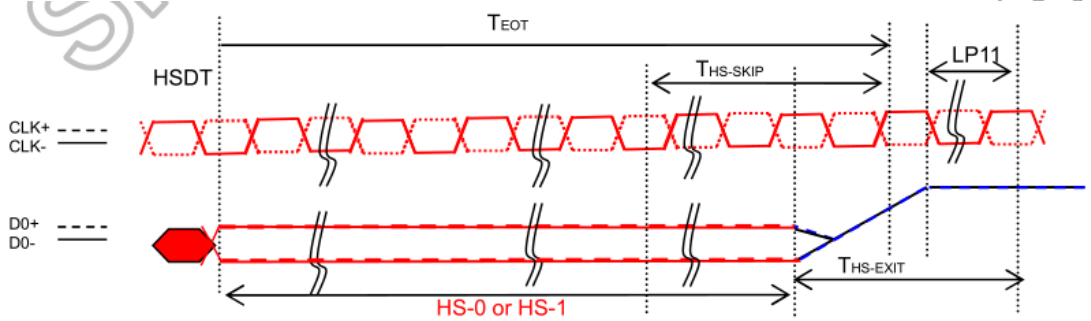
Table : DSI Low Power Mode characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

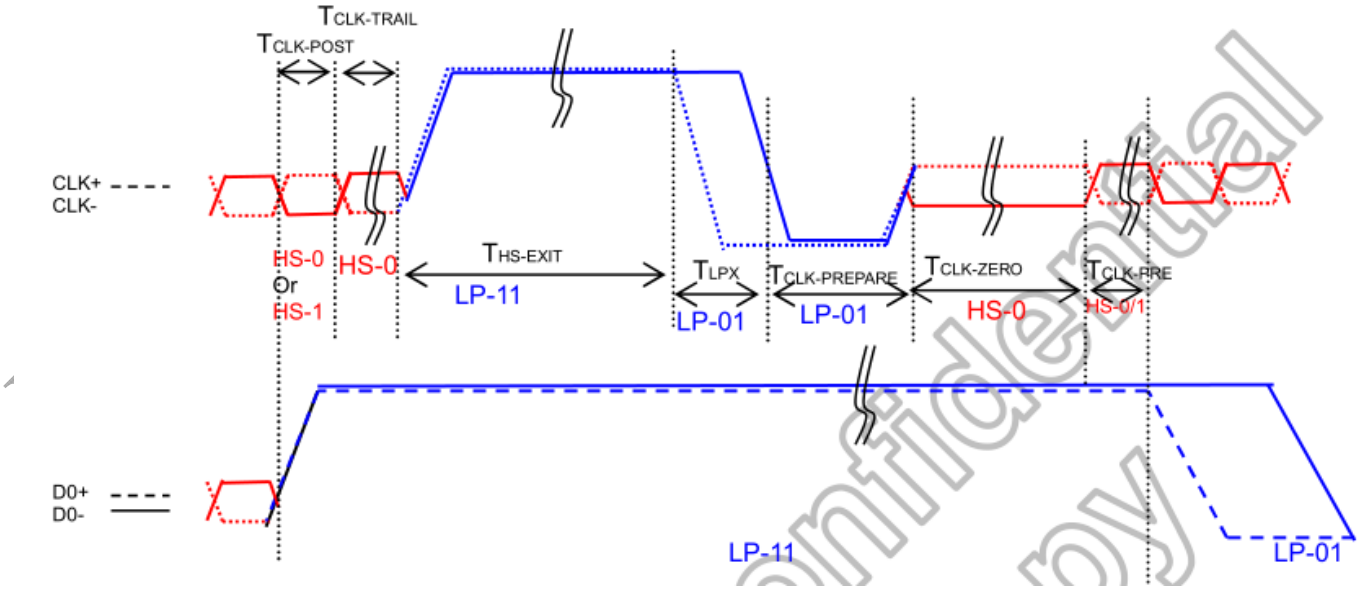
Table : DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table : DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table : Clock Lanes High Speed Mode to/from Low Power Mode Timings

5.3 Reset input timing

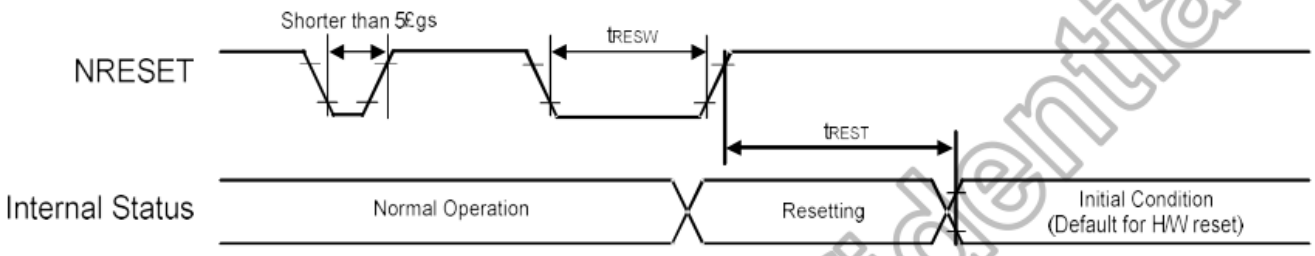


Figure : Reset input timing

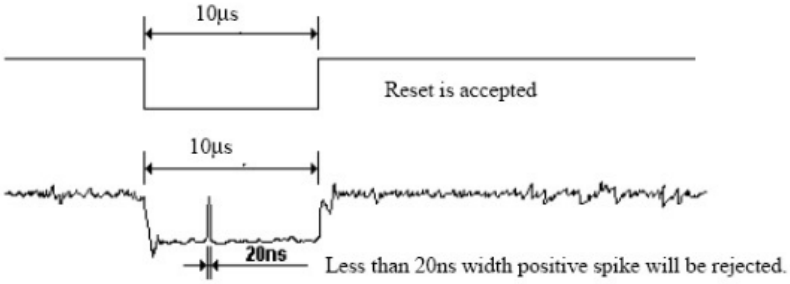
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table : Reset input timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown as below:

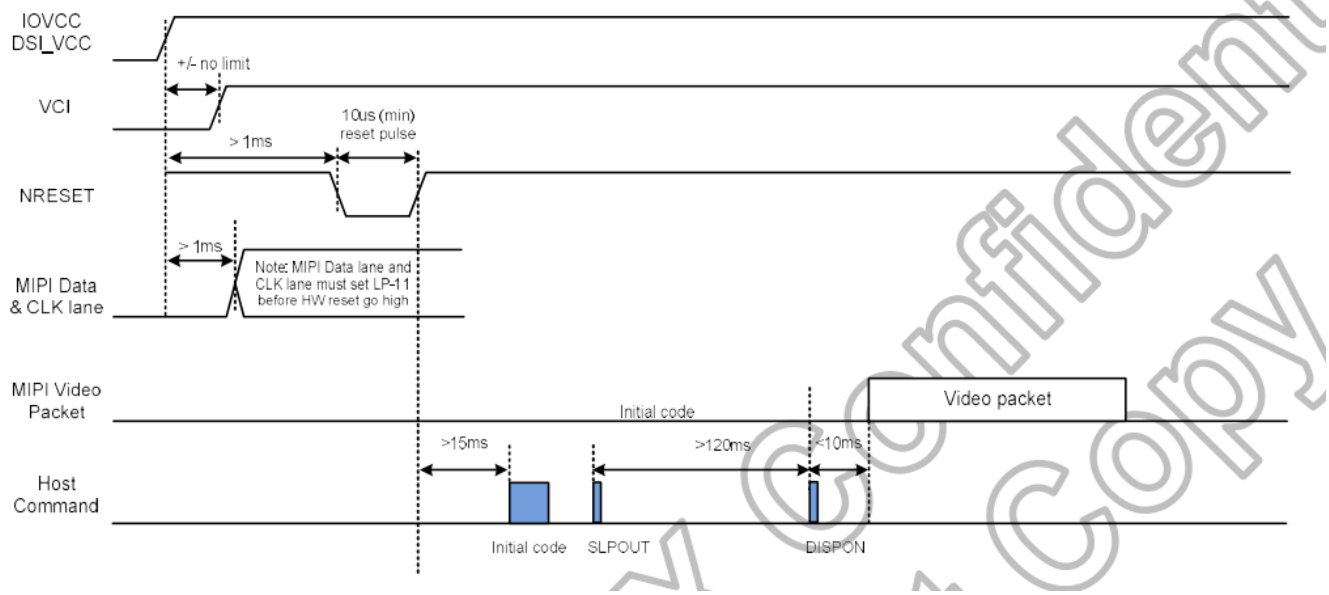


(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

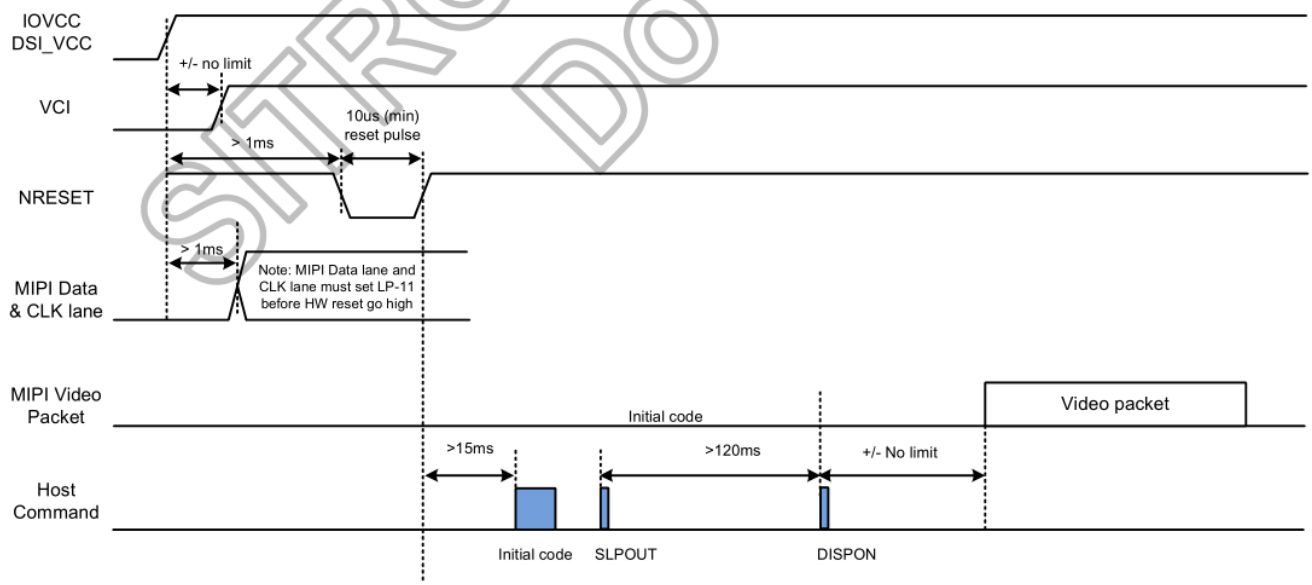
5.4 DSI POWER ON/OFF TIMING

5.4.1 Power on Timing

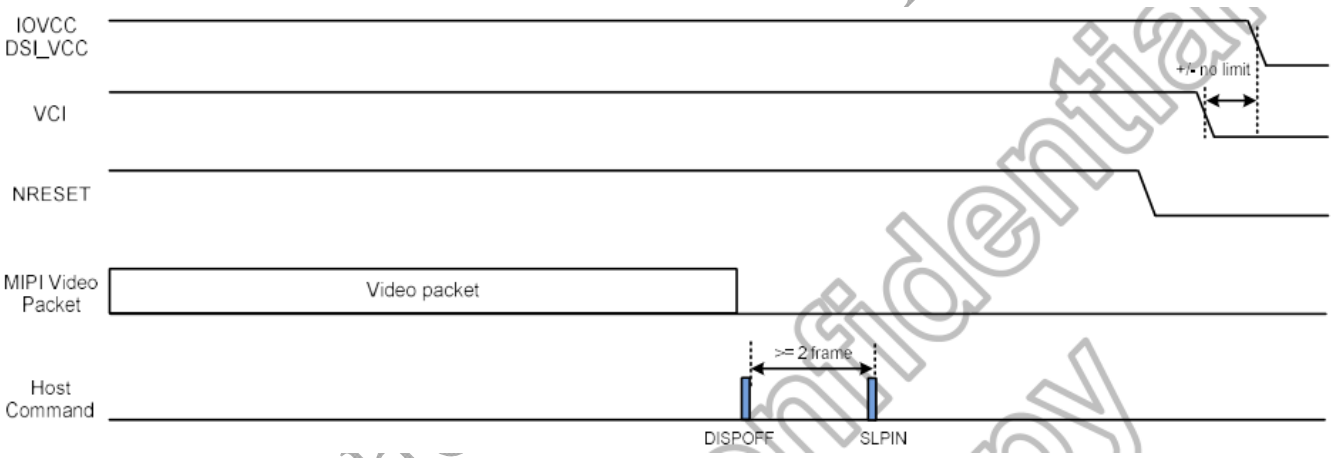
ESD_WHITE_EN=0



ESD_WHITE_EN=1



5.4.2 Power off Timing



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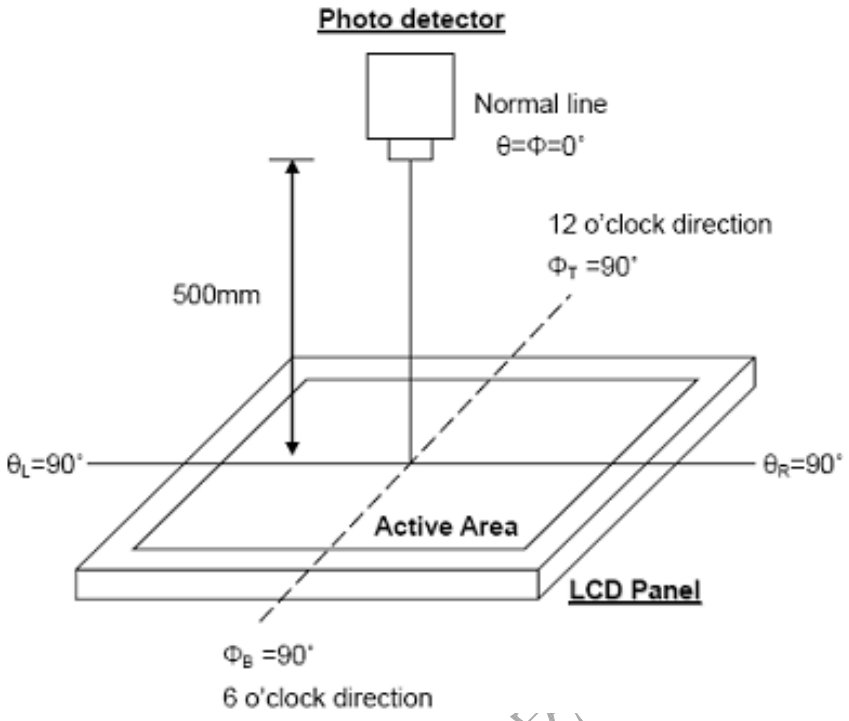
6.OPTICAL CHARACTERISTICS

Ta=25±2℃

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	800	1000	-		Note1 Note4
Luminance		YL	400	450	-	cd/m2	Note1 Note6 Note7
Luminous Uniformity		IV-M	75	80		%	
Response Time (Rising + Falling)		T_{RT}	-	30	35	ms	Note1 Note3
Viewing Angle range	Horizontal	θ_L	-	80	-		Note2
		θ_R	-	80	-		
	Vertical	θ_U	-	80	-		
		θ_D	-	80	-		
Color Chromaticity	Red	x	-0.03	0.644	+0.03		Note1 Note5 Note7
		y		0.334			
	Green	x		0.308			
		y		0.626			
	Blue	x		0.146			
		y		0.052			
	White	x		0.265			
		y		0.315			
Color Gamut				70		%	

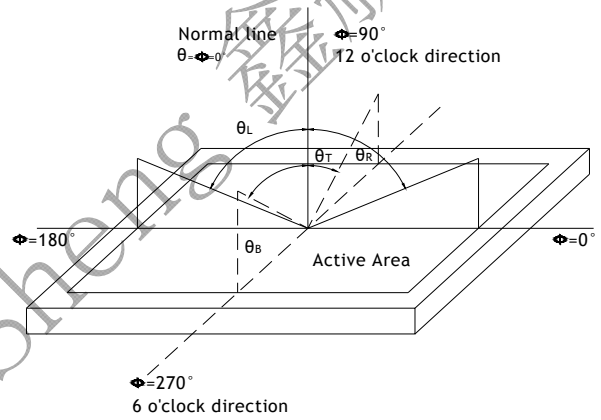
Note1: Definition of optical measurement system (BM-7)

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Note2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.

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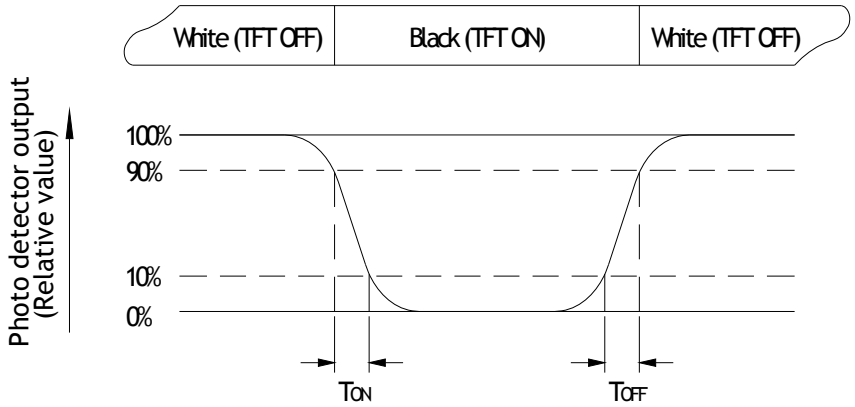


Fig. 6-3 Definition of response time

Note4: Definition of contrast ratio

Contrast ratio(CR)=错误！未找到引用源。

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

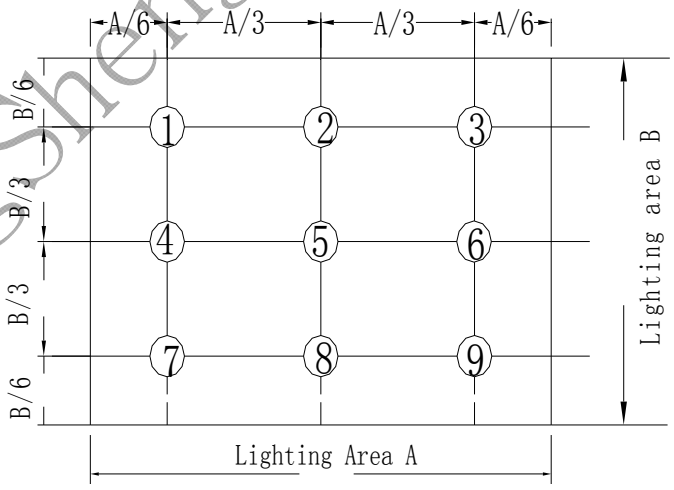
Note6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IL=260mA

Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas.Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L----Active area length, W---- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

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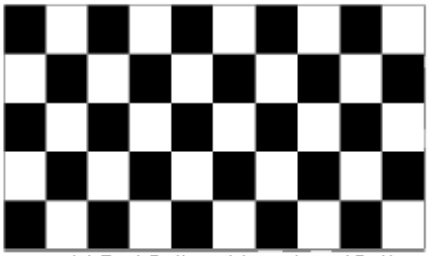
7.RELIABILITY TEST ITEMS

7.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition	Criterion
High Temperature Storage	80℃±2℃ 120H Restore 2H at 25℃ Power off	IEC60068-2-12007 GB2423.2-2008
Low Temperature Storage	-30℃±2℃ 120H Restore 2H at 25℃ Power off	IEC60068-2-12007 GB2423.2-2008
High Temperature Operation	70℃±2℃ 120 H Restore 2H at 25℃ Power on	IEC60068-2-12007 GB2423.2-2008
Low Temperature Operation	-20℃±2℃ 120 H Restore 2H at 25℃ Power on	IEC60068-2-12007 GB2423.2-2008
High Temperature & Humidity Operation	60℃±2℃ 90%RH 120H Power on	IEC60068-2-12001 GB2423.3-2006
Temperature Cycle	-20℃←→70℃ 30min 30min after 24cycle, Restore 2H at 25℃ Power off	IEC60068-2-14:1984, GB2423.22-2002
Vibration Test	10Hz~45Hz, 100m/s2, 120min	
Shock Test	Half-sinewave,300m/s2,11ms	
Drop Test(package state)	Height 600mm,concretefloor, 1corner,3edges, 6 surfaces.	1.After testing, cosmetic and electrical defects should not happen. 2.the product should remain at initial place 3.Product uncovered or package broken is not permitted.
Electro Static Discharge Test (non-operation)	150pF，330Ω，Contact:±4KV,Air: ±8KV Measure point :LCD glass and metal bezel 200pF，0Ω，±200V contact test Measure point :IF connector pins	IEC61000-4-2： 2001 GB/T17626.2-2006
Image Sticking @ Room Temp.	25 ℃；1 hrs	Note1: 6*8 check pattern，25 ℃±2 ℃；Aging Time:1hrs; Recovery Time:5min @127/2 56 Gray Level

Note1:Condition of image sticking test :25℃±2℃
Operation with test pattern sustained for 1hrs,then change to gray pattern immediately.after 15 mins,the mura must be disappeared completely

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(a) Test Pattern (chess board Pattern)


(b) Gray Pattern

7.2 VIBRATION&SHOCK

Test item	Conditions	Remark
Packing Shock (non-operation)	980m/s2,6ms, ±x,y,z 3times for direction	IEC60068-2-27：1987 GB/T2423.5-1995
Packing Vibration (non-operation)	Frequency range:10 HZ~50HZ Stroke:1.0mm,sweep:10 HZ ~50HZ x,y,z 2 hours for each direction	IEC60068-2-32：1990 GB/T2423.8-1995

7.3ESD

Test item	Conditions	Remark	
Electro Static Discharge Test (non-operation)	150pF，330Ω， Contact:±2KV,Air:±4KV	1	Class C
	200pF，0Ω，±200V contact test	2	

Note: Measure point :
1. LCD glass and metal bezel
2. IF connector pins
3. ESD class C: To allow a temporary loss of function, the equipment to be measured may stop working but should be able to automatic or manual intervention reset back to normal after operation.

8. GENERAL PRECAUTION

8.1 SAFETY

1. Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
2. If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
3. If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

1. Store the panel or module in a dark place where the temperature is 23±5° C and The humidity is below 50±20%RH.
2. Store in anti-static electricity container.
3. Store in clean environment, free from dust, active gas, and solvent.
4. Do not place the module near organics solvents or corrosive gases.
5. Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

1. Avoid static electricity which can damage the CMOS LSI.
2. The polarizing plate of the display is very fragile. So, please handle it very carefully.
3. Do not give external shock.
4. Do not apply excessive force on the surface.
5. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the Surface of plate.

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6. Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
7. Do not operate it above the absolute maximum rating.
8. Do not remove the panel or frame from the module.
9. When the module is assembled, it should be attached to the system firmly, Be careful not to twist and bend the module.
10. Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.
11. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth in case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

8.4 WARRANTY

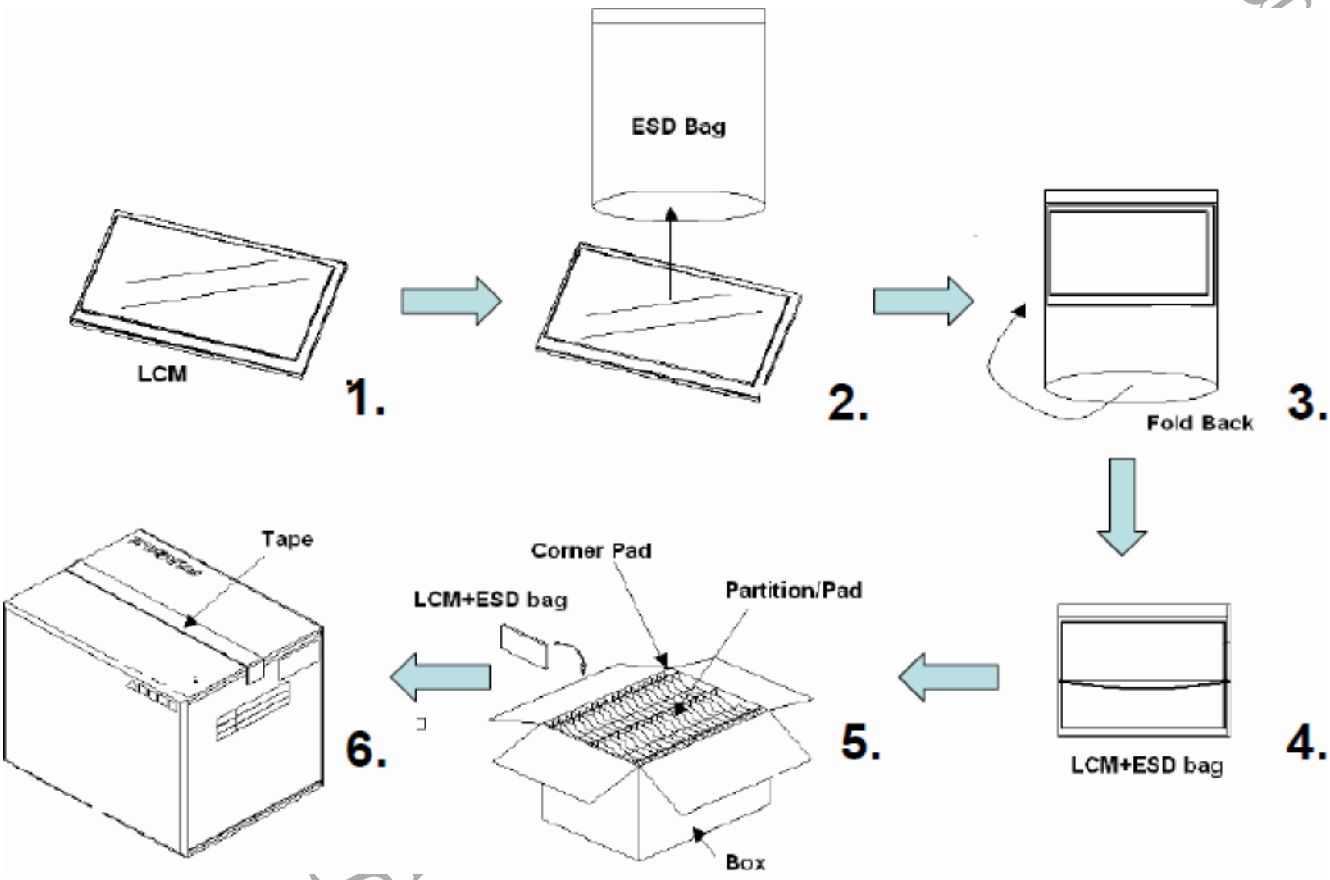
1. The period is within twelve months since the date of shipping out under normal using and storage conditions.
2. Do not repaired or modified the LCM. It may cause function to lose efficacy, Starry does not warrant the LCM.
3. All process and material comply ROHS.

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9. PACKAGE DRAWING

Packing form

LCM Model	LCM Qty. in the box	Inner Box Size (mm)	Notice
WD090HBM30AC-S0-07	50 pcs/box	383±5 x 373±5 x 275±5	



Items	Material	Notice
Box	Corrugated Paper Board	AB Flute
Partition/Pad	Corrugated Paper Board	B Flute
Corner Pad	Corrugated Paper Board	AB Flute
ESD bag	PE	

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INCOMING INSPECTION STANDARDS

MODEL: WD090HBM30AC-S0-07

<◇>PRELIMINARY SPECIFICATION

<◆>APPROVAL SPECIFICATION

DESIGNED	CHECKED	APPROVED

DESIGNED	CHECKED	APPROVED

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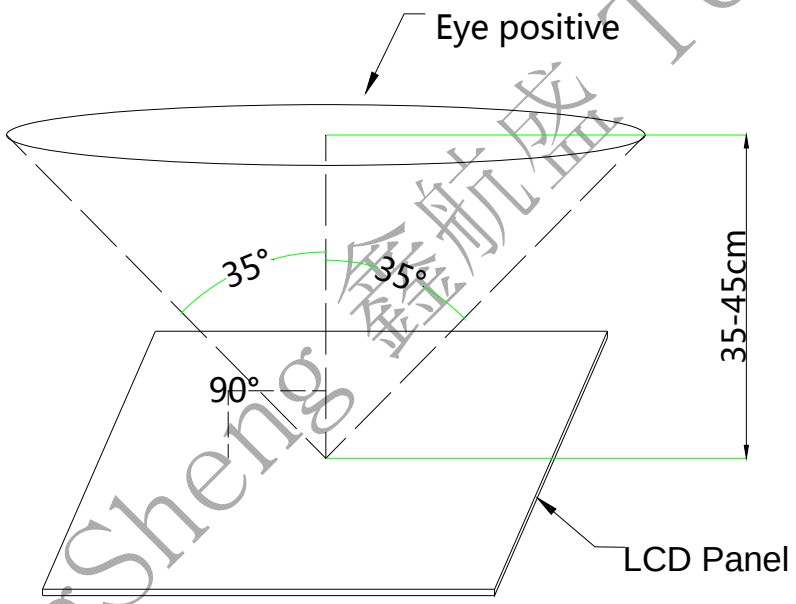
PREPAREDBY:
XINHANGSHENG TECHNOLOGY (SHENZHEN) CO., LTD.
2 BUILDING, 10 HIGH TECH PARK OF BAO TONG, TONGWEI, COMMUNITY GONGMINGTOWN,GUANGMING DISTRICT,
SHENZHEN,GUANGDONG,CHINA
TEL : +86-755-23400464
Mobile : +86-18682352622

1. Incoming inspection right

(1) The Incoming Inspection Standard will be agreed and signed by both sides(Customer an starry)

2. Inspection condition is as follows

(1) Viewing distance is approximately 30 cm
(2) Viewing angle is normal to the LCD panel as Fig-1(35°)
(3) Ambient temperature is approximately 25±5℃
(4) Ambient illumination: 1000±200 Lux for Sheet appearance inspection
(5) Ambient illumination: 100±50 Lux for shorting bar test.
(6) B/L brightness is 2000±200cd/m ^{2}



3. Special condtion

(1) Viewing distance is close for inspection of adjacent dots and distance between defect Dots
(2) Viewing condition of " Shot block non-uniformity from oblique angle"is as Fig-2
(3) Exceptional case:Veiw angle±40° while inspected image-sticking

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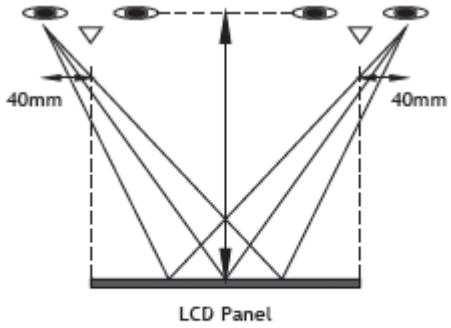
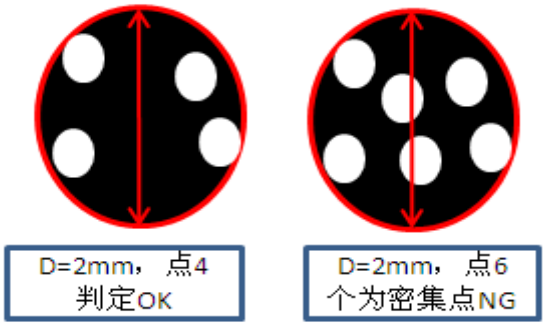


Fig-2

4. INSPECTION CRITERIA

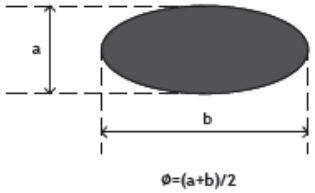
Defecttype			Limit			Note
Visual defect	Scratch		W≦0.05mm		lgnore	Note1
			0.05mm≦w≦0.1m L≦10mm		N≦3	
			20mm < l，0.1mm < w		N=0	
	Internal	Spot	Φ < 0.2mm		lgnore	Note 1
			0.2mm≦φ≦0.3mm		N≦2	
			0.3≦φ		N=0	
		Fiber	0.1mm≦w≦0.2mm L≦1.5mm		N≦2	Note 1
			0.2mm < w，2.5mm < l		N=0	
		Polarizer bubble	Φ < 0.15mm		lgnore	Note 1
			0.15mm≦φ≦0.3mm		N≦2	
			0.35≦φ		N=0	
		Dent	Φ < 0.25mm		lgnore	Note 1
			0.25mm≦φ≦0.5mm		N≦3	
			0.5≦φ		N=0	
Electrical Defect	Bright dot		C area	O area	Total	Note 2 Note 3 use of ND5 % invisible OK
			N≦1	N≦2	N≦3	
	Dark dot		N≦2	N≦4	N≦4	
	Total dot		N≦3	N≦4	N≦4	

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	Dense point	Using ND5 % visible by intensive foreign standard judgement, ND5 % invisible OK  	Note 4

(1) One pixel consists of 3 sub-pixel,including r,g,ang b dot.(sub-pixel=dot)
(2) Panel is acceptable if distance between 2 dot defects are greater or equal to 5mm.

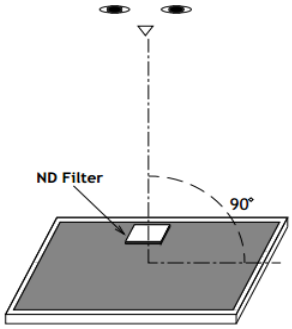
Note1 : W : Width[mm], L : Length[mm], N : Number, φ: Average Diameter

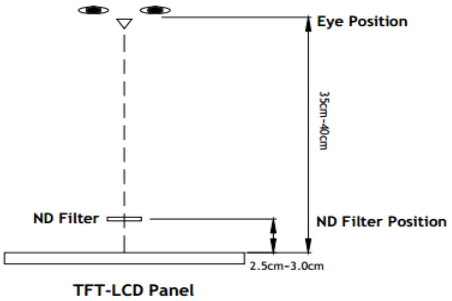


1.(White ,Black) Spot
2.Polarizer Bubble

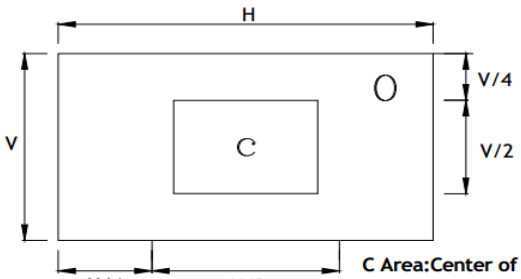


Scratch & Fiber



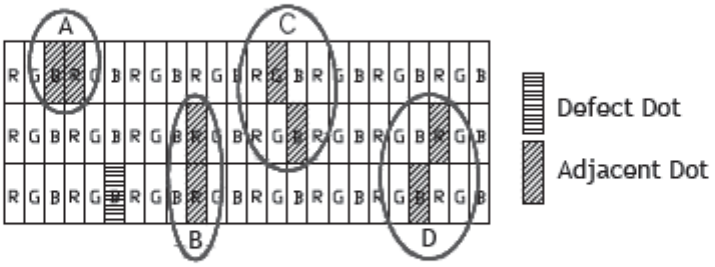


Note3 :



C Area:Center of display area
O Area:Outer of display area

Note4：Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dart adjacent dot. And they will be counted 2defect dots in total quantity.



Note5：Other condition

(1) The defects that are not defined above and considered to be problem shall be reviewed anddiscussed by both parties.

(2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

5.HADLING PRECAUTION

(1)Don't disassemble and reassemble the module by self
(禁止自行拆解)

(2)Acid,alkali,alcohol or touched directly by hand will damage the display.
(酸性、碱性、酒精或手的直接接触将会损伤显示面)

(3)Static electricity will damage the module.Please configure grounding device.
(静电会损伤模组，请装配接地设备)

(4)The strong vibration,shock,twist or bend will cause material damage,even module broken.
(强烈的撞击、震动、扭转或弯曲将会造成原材损伤，甚至面板破裂)

(5)It is easy to cause image sticking while displaying the same pattern for very long time.
(长期显示同一画面会造成影像残留)

(6)The response time,brightness and performance will vary from different temperature.
(响应时间、亮度与均匀性会因温度而有所改变)

(7)The Period within 12 months since the date of shipping out under normal using And Storage conditions.
(从出货之日开始,在正常使用和存储条件下,产品保质期为12个月)

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